UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/902,170	07/11/2001	Masahiko Ando	H6810.0011/P011	8805

24998 7590 11/06/2002

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER
NGUYEN, KHIEM D

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/902,170	ANDO ET AL.	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication app ars on the cover sh t with the correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-98* is/are pending in the application.

4a) Of the above claim(s) *35-49 and 84-98* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34 and 50-83* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of claims 1-34 and 50-83 in Paper No. 7 is acknowledged. The traversal is on the ground(s) that, the applicants respectfully submit that all of the claims can be searched and examined together without serious burden. This is not found persuasive because inventions of method group (I), claims 1-34 and 50-83 and device group (II), claims 35-49 and 84-98 have different classifications so the searches are non-coextensive. Further, the examiner has shown that the process of removing impurity from the channel region can be perform by an RCA cleaning method instead of using a plasma chemical vapor deposition apparatus. See the restriction. The requirement is still deemed proper and is therefore made FINAL.

Drawings

Figure 6(a)-(d) should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 11 is objected to because of the following informalities: In Claim 11, delete "formed" insert "form". Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 13, and 24 recite the limitation "amorphous silicon layer" in line 7. There is insufficient antecedent basis for this limitation in the claim.

Claims 50, 62 and 73 recite the limitation "amorphous silicon layer" in line 10. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art of this application (AAPA) in view of Ting (U.S. Patent 6,214,705) and Washizuka et al. (IDW 1997 pp. 207-210).

AAPA teaches a method of fabricating a thin film transistor comprising the steps of (See Discussion of the Related Art on page 1-2 of this application and FIG. 6(a)-(d)):

providing a gate 62 over a substrate 61;

providing a gate insulating layer 63 over the gate and substrate;

providing an amorphous silicon layer 64 having a high resistance over the gate insulating layer;

providing an impurity 65 over the amorphous silicon layer;

forming a drain electrode 66 and source electrode 67 separated by a channel region over a contact portion with the amorphous silicon; and,

removing the impurity from the channel region to form a contact layer wherein the contact layer has a resistance at least lower than the first resistance.

AAPA fails to teach diffusing the impurity into the contact portion by an annealing process wherein the annealing is conducted at a temperature of about 300°C-320°C for about 10-15 minutes and wherein the impurity is phosphorus as recited in present claims 5-7, 17-19 and 28-30.

Ting teaches diffusing the impurity into the amorphous silicon layer by an annealing process (See col. 3, lines 7-10) wherein the impurity is phosphorus (See col. 2, lines 62-66). It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to incorporate Ting's teaching into AAPA's method because in doing so can lower the resistance of the gate electrode (See col. 3, lines 4-6).

Ting fails to teach the annealing temperature and time duration as recited in present claims 6, 18, and 29. However, the annealing temperature and time duration are result-effective variables and there is no evidence indicating that the annealing temperature and time duration are critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

AAPA fails to teach the thickness of the amorphous silicon film, the concentration of the impurity, and the exposure time as recited in present claims 2, 4, 8, 14, 16, 20, 25, 27, and 29. However, it has been held that it is not inventive to discover the optimum or workable thickness, concentration of the impurity, and the exposure time

of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

AAPA fails to teach removing the impurity from the channel region is performed by exposure to hydrogen plasma as recited in present claims 3, 15, and 26. However, the process of removing the impurity by expose to hydrogen plasma is well-known to ***one of ordinary skill in the art of making semiconductor devices.***

AAPA fails to explicitly teach that the diffusing step is performed simultaneously with an annealing step for a capping layer provided over the electrodes and the channel region as recited in present claims 9, 21, and 32. However, selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results. In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

AAPA fails to teach wherein the amorphous silicon layer is etched utilizing a common photoresist used to form the electrodes as recited in present claims 11, 13 and 24.

Washizuka teaches etching the amorphous silicon layer utilizing a common photoresist used to form the electrodes (See page 208 and FIG. 3). It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to incorporate Washizuka's teaching into AAPA's method in order to achieve high image quality of TFT-LCDs (See page 207).

4. Claims 50-83 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art of this application (AAPA) in view of Ting (U.S. Patent 6,214,705) and Washizuka et al. (IDW 1997 pp. 207-210).

AAPA teaches a method of fabricating a liquid crystal display (LCD) comprising the steps of (See Discussion of the Related Art on page 1-2 of this application and FIG. 6(a)-(d)):

providing a plurality of thin film transistors arranged on a LCD substrate in a matrix form, each of the thin film transistors fabricated by the steps of:

providing a gate 62 over a substrate 61;

providing a gate insulating layer 63 over the gate and substrate;

providing an amorphous silicon layer 64 having a high resistance over the gate insulating layer;

providing an impurity 65 over the amorphous silicon layer;

forming a drain electrode 66 and source electrode 67 separated by a channel region over a contact portion with the amorphous silicon; and,

removing the impurity from the channel region to form a contact layer wherein the contact layer has a resistance at least lower than the first resistance.

AAPA fails to teach diffusing the impurity into the contact portion by an annealing process wherein the annealing is conducted at a temperature of about 300°C-320°C for about 10-15 minutes and wherein the impurity is phosphorus as recited in present claims 54-56, 66-68, and 77-79.

Ting teaches diffusing the impurity into the amorphous silicon layer by an annealing process (See col. 3, lines 7-10) wherein the impurity is phosphorus (See col. 2, lines 62-66). It would have been obvious to ***one of ordinary skill in the art of making***

semiconductor devices to incorporate Ting's teaching into AAPA's method because in doing so can lower the resistance of the gate electrode (See col. 3, lines 4-6).

Ting fails to teach the annealing temperature and time duration as recited in present claims 55, 67, and 78. However, the annealing temperature and time duration are result-effective variables and there is no evidence indicating that the annealing temperature and time duration are critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

AAPA fails to teach the thickness of the amorphous silicon film, the concentration of the impurity, and the exposure time as recited in present claims 51, 53, 57, 63, 65, 69, 74, 76, and 80. However, it has been held that it is not inventive to discover the optimum or workable thickness, concentration of the impurity, and the exposure time of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

AAPA fails to teach removing the impurity from the channel region is performed by exposure to hydrogen plasma as recited in present claims 52, 64, and 75. However, the process of removing the impurity by expose to hydrogen plasma is well-known to ***one of ordinary skill in the art of making semiconductor devices.***

AAPA fails to explicitly teach that the diffusing step is performed simultaneously with an annealing step for a capping layer provided over the electrodes and the channel region as recited in present claims 58, 70, and 81. However, selection of any order of

performing process steps is prima facie obvious in the absence of new or unexpected results. In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

AAPA fails to teach wherein the amorphous silicon layer is etched utilizing a common photoresist used to form the electrodes as recited in present claims 60, 62, and 73.

Washizuka teaches etching the amorphous silicon layer utilizing a common photoresist used to form the electrodes (See page 208 and FIG. 3). It would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to incorporate Washizuka's teaching into AAPA's method in order to achieve high image quality of TFT-LCDs (See page 207).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaudhuri Olik can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-9179 for regular communications and (703) 746-9179 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
October 31, 2002

Supervisory Patent Examiner
Technology Sector 2800